

SPECIFICATION

LOGIC CIRCUIT WITH RESTRAINED LEAK
CURRENT TO DIFFERENTIAL CIRCUIT

5

TECHNICAL FIELD

[0001]

The present invention relates to logic circuits such as a latch circuit

10 BACKGROUND ART

[0002]

There is known a latch circuit which comprises a differential circuit as a basic element circuit of logic circuits used in a variety of semiconductor integrated circuits.

15 [0003]

Fig. 1 illustrates a circuit diagram of a conventional general latch circuit. As illustrated in Fig. 1, conventional latch circuit 50a comprises a vertical stack for a total of three stages which include a differential circuit (a differential pair composed of transistors Q51 and Q52 and the like) stage for reading data and a differential circuit (a differential pair composed of transistors Q53 and Q54 and the like) stage for holding data; a differential circuit (a differential pair composed of transistors Q55, Q56 or the like) stage which receives a clock signal and which functions to switch a current to an upper stage of the differential circuit; and a stage of transistor Q57, at a lower stage than that, for regulated current source.

[0004]

Thus, the foregoing configuration requires a higher supply voltage, as compared with other basic circuit elements, and constitutes an impediment to a total reduction in voltage and power consumption when the logic circuit is integrated into one chip or a modular form together with other functional circuit blocks. Consequently, a large challenge has been to restrain power consumption of the latch circuit (see, for example, JP-A-63-86611 and JP-A-2-21717).

[0005]

As a measure to reduce voltage for such a latch circuit, a circuit as illustrated in Fig. 2, for example, is proposed in JP-A-63-86611 and JP-A-2-21717.

[0006]

Fig. 2 illustrates a circuit diagram of a latch circuit which has two differential circuits arranged in parallel (parallelly arranged latch circuit). In latch circuit 50b illustrated in Fig. 2, a current switching transistor (Q58), which is applied with a clock signal, has an emitter terminal connected to a common emitter terminal of a differential circuit (composed of transistors Q51 and Q52 and the like), while a current switching transistor (Q59) has an emitter terminal connected to a common emitter terminal of a differential circuit (composed of transistors Q53 and Q54 and the like).

[0007]

In such a circuit configuration, only if logical amplitudes are set high for the current switching transistors (Q58, Q59) will a current to the differential circuits be shut off when the clock signal is at a high level because current from a regulated current source flows through the current switching transistors (Q58, Q59). On the other hand, when the clock signal

is at a low level, the current from the regulated current source flows through the differential circuits.

[0008]

In the foregoing manner, in the circuit illustrated in Fig. 2, a latching 5 operation is implemented by switching a current in synchronization with the clock. In this way, the need to arrange a vertical stack of differential circuits is eliminated, thus making it possible to reduce the voltage.

[0009]

However, the conventional circuit has problems shown below.

10 [0010]

So that latch circuit 50b as illustrated in Fig. 2 operates correctly, a strong influence on the switching operate under control of the clock signal must be increased, as compared with data signals, such that currents from current source transistors (Q60, Q61) will always flow through the current 15 switching transistors (Q58, Q59) when the clock signal is at a high level.

This can be made possible by setting the size of the current switching transistors (Q58, Q59) larger than the transistors (Q51, Q52, Q53, Q54) which made up the differential circuits. As the size of the transistors (Q58, Q59) is larger, the strong influence of the clock signal is increased.

20 However, the use of excessively large transistors would result in a degradation in high-speed performance and an increase in consumed current.

[0011]

Thus, there are limitations in the size of the current switching 25 transistors (Q58, Q59) per se, so that it is actually difficult to completely have a strong influence on the current switching transistors (Q58, Q59). For this

reason, even when the clock signal is at a high level, part of the current supplied from a current source will leak to the differential circuits.

[0012]

- Fig. 3 is a diagram representing the relationship between current I1 which flows into a current switching transistor and current I2 which flows into a differential circuit from a current source in a parallelly arranged latch circuit when it is in operation. It can be seen that when the current switching transistor (Q58) turns on to allow I1 to flow, current I2 to the differential circuit, which should be essentially shut off, is not completely eliminated (portion A in the figure), but a leak current flows. A reduction in potential level of a data signal due to this leak current can lead to a degradation in output waveform and the like, if the reduction is not negligible with respect to a logical amplitude of data.

[0013]

- Also, irrespective of the type of circuit forms that make up latch circuits, generally, when an attempt is made to reduce a supply voltage, VCE distributed to each transistor cannot but be reduced. For this reason, an optimal operating condition cannot always be selected for high frequency performance of a device, thus leading to difficulties in ensuring high-speed performance. As a measure to improve high speed performance, an inductor keeping technique is effective.

[0014]

- Fig. 4 illustrates a circuit diagram of a parallelly arranged latch circuit which has improved high-speed performance. To improve high-speed performance, a wire is extended on a collector side of a differential circuit (transistors Q51 and Q52 or transistors Q53 and Q54), or a spiral inductor is

disposed on the collector side. Based on parallel resonance of inductance L produced herein and capacitance C of a transistor connected at the next stage, the gain is increased in a high frequency region to improve high-speed performance.

5 [0015]

Incidentally, in regard to a parallelly arranged latch circuit, the improvement in high-speed performance is desirable for the current switching transistors (Q58, Q59) as well, except for the differential circuit. However, in the example of Fig. 4, the collectors of the current switching 10 transistors (Q58, Q59) are simply connected to a high potential power supply terminal through resistors, but circuits including transistors are not at all connected, so that a capacitive component in this portion is nothing but an extremely small stray capacitance. Thus, for giving rise to gain peaking based on parallel resonance in a desired high frequency region, an 15 extremely large wiring inductance is required, thereby making improvement in high-speed performance unrealistic due to restraints in the chip area.

[0016]

A large number of latch circuits are used in a variety of functional circuits. Fig. 5 is a diagram illustrating circuit blocks of 2:1 MUX. As 20 illustrated in Fig. 5, 2:1 MUX comprises circuit elements such as master/slave flip-flop circuit (MS-F/F) 71, master/slave/master flip-flop circuit (MSM-F/F) 72, selector circuit (SELECTOR) 73, and the like. Each of these circuit elements is built using latch circuits. Here, since complementary clock signals are supplied to each circuit element, the clock signal is 25 branched into a large number of paths. For this reason, a buffer circuit is required in each branch for signal amplification, resulting in an increased

number of circuits and increased power consumption. Therefore, in integrated functional circuits, it is necessary not only to reduce power consumption of respective latch circuits, but also to reduce the number of circuits such as buffer circuits (BUF).

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DISCLOSURE OF THE INVENTION

[0017]

It is an object of the present invention to provide a logic circuit such as a latch circuit, selector circuit and the like, which excels in a low voltage, low power consumption, and high-speed performance by mainly restricting a leak current to a differential circuit.

[0018]

To achieve the above object, in the present invention, a logic circuit is provided therein with a current supply control circuit for controlling the amount of current supplied to a differential circuit. This current supply control circuit comprises a bypass path for bypassing the current around the differential circuit, a switching transistor interposed in the bypass path for opening/closing the bypass path in accordance with the signal level of a clock applied from the outside, and a current amount control transistor for controlling the amount of current supplied to the differential circuit. The current amount control transistor adjusts the amount of current in accordance with the signal level of the clock signal. The current amount control transistor is configured to ensure a sufficient amount of current when current flows into the differential circuit in response to the clock signal, and to thoroughly reduce an amount of current when current flows into the bypass circuit, thus reducing the amount of current leaking to the differential circuit

when a current flows into the bypass circuit.

[0019]

According to the present invention, since the amount of current supplied to the differential circuit is adjusted in accordance with the signal

5 level of the clock signal, unwanted leak current can be automatically restrained from flowing into the differential circuit. Also, by using such a configuration, the size of transistors used in the logic circuit can be reduced in order to increase speed and reduce power consumption.

10 BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

[Fig. 1]

A circuit diagram of a general latch circuit in the prior art.

[Fig. 2]

15 A circuit diagram of a prior art latch circuit (parallelly arranged latch circuit) which has two differential circuits arranged in parallel.

[Fig. 3]

A graph representing the relationship between current I1 which flows into a current switching transistor and current I2 which flows into a differential

20 circuit from a current source in the latch circuit of Fig. 2 when it is in operation.

[Fig. 4]

A circuit diagram of a parallelly arranged latch circuit in the prior art which has improved high-speed performance.

25 [Fig. 5]

A circuit block diagram of prior art 2:1 MUX.

[Fig. 6]

A circuit diagram of a latch circuit according to a first embodiment of the present invention.

[Fig. 7A]

5 A circuit diagram of a latch circuit according to a second embodiment of the present invention.

[Fig. 7B]

A circuit diagram illustrating details of voltage control circuits 18, 19 in the latch circuit of Fig. 7A.

10 [Fig. 8A]

A graph representing the manner in which current I1 flowing through a bypass path and current I2 flowing through a differential pair vary in synchronization with variations in the clock level (signal level) of a clock signal in latch circuit 1b of Fig. 7B.

15 [Fig. 8B]

A graph representing variations in the clock level (signal level) of the clock signal.

[Fig. 9A]

20 A circuit diagram of a master/slave D-type F/F circuit which employs the latch circuit of Fig. 7B and is used in an identifier and the like (when voltage control circuits 18, 19 are provided individually).

[Fig. 9B]

A circuit diagram of a master/slave D-type F/F circuit which employs the latch circuit of Fig. 7B and is used in an identifier and the like (when voltage control circuits 18, 19 are shared).

[Fig. 10A]

A circuit diagram of a latch circuit according to a third embodiment of the present invention.

[Fig. 10B]

- A circuit diagram illustrating details of level shift circuits 24, 25 in the
5 latch circuit of Fig. 10A.

[Fig. 11A]

A circuit diagram of a latch circuit according to a fourth embodiment of the present invention.

[Fig. 11B]

- 10 A circuit diagram illustrating details of circuits 26, 27 including capacitance C in the latch circuit of Fig. 11A.

[Fig. 12A]

A circuit diagram of a latch circuit according to a fifth embodiment of the present invention.

- 15 [Fig. 12B]

A circuit diagram illustrating details of circuits 26, 27 including capacitance C in the latch circuit of Fig. 12A.

[Fig. 13]

- 20 A circuit diagram of a latch circuit according to a sixth embodiment of the present invention.

[Fig. 14A]

A circuit block diagram of 2:1 MUX which is built using latch circuit 5 of Fig. 13.

[Fig. 14B]

- 25 A circuit block diagram of a circuit which is built using latch circuit 5 of Fig. 13.

[Fig. 15]

A circuit diagram of a selector circuit according to the present invention.

5 **BEST MODE FOR CARRYING OUT THE INVENTION**

[0021]

(First Embodiment)

Referring first to Fig. 6, a description will be given of the configuration of a latch circuit according to a first embodiment of the present invention.

10 [0022]

Fig. 6 illustrates a circuit diagram of the latch circuit according to the first embodiment of the present invention. In Fig. 6, 11a and 11b designate data signal input terminals; 12a and 12b data signal output terminals; 13a and 13b clock signal input terminals; 14 a high potential power supply terminal which is supplied with potential Vcc; and 15 a low potential power supply terminal which is supplied with potential Vee.

[0023]

For reference purposes, a data signal applied to data signal input terminal 11b is a data complementary signal, the signal (logical) level of which is inverted from that of a data signal applied to data signal input terminal 11a. Also, a clock signal applied to clock signal input terminal 13b is a complementary clock signal, the signal level of which is inverted from that of a clock signal applied to clock signal input terminal 13a.

[0024]

25 As illustrated in Fig. 6, latch circuit 1a of the first embodiment includes data reading differential pair 16 as a first differential circuit for reading data

signals applied from data signal input terminals 11a and 11b; data holding differential pair 17 as a second differential circuit for holding the data signals; voltage control circuit 18 and current source transistor Q7 as first control means for controlling the amount of current supplied to data reading

- 5 differential pair 16; voltage control circuit 19 and current source transistor Q8 as second control means for controlling the amount of current supplied to data holding differential pair 17; first bypass path 20 for bypassing current around data reading differential pair 16; second bypass path 21 for bypassing current around data holding differential pair 17; current switching
- 10 transistor Q5 as first switching means for opening and closing first bypass path 20 in accordance with the signal level of the clock signal applied from clock signal input terminal 13a; and current switching transistor Q6 as second switching means for opening and closing second bypass path 21 in accordance with the signal level of the complementary clock signal applied
- 15 from clock signal input terminal 13b.

[0025]

For reference purposes, bypass path 20, current switching transistor Q5, voltage control circuit 18, and current source transistor Q7 (or bypass path 21, current switching transistor Q6, voltage control circuit 19, and

- 20 current source transistor Q8) function as a current supply control circuit of the present invention.

[0026]

Data reading differential pair 16 includes transistors Q1 and Q2, wherein transistor Q1 has a collector (terminal) connected to high potential power supply terminal 14 through resistor R1, while transistor Q2 has a collector connected to high potential power supply terminal 14 through

resistor R2. Also, the collector of transistor Q1 is connected to data signal output terminal 12a, and the collector of transistor Q2 is connected to data signal output terminal 12b, respectively. As well, transistor Q1 has a base (terminal) connected to data signal input terminal 11a, and transistor Q2 has

5 a base connected to data signal input terminal 11b, respectively. Also, a common emitter of data reading differential pair 16, i.e., an emitter connection point of transistors Q1 and Q2, is connected to an emitter (terminal) of current switching transistor Q5 and to a collector of current source transistor Q7.

10 [0027]

Further, current switching transistor Q5 has a collector connected to high potential power supply terminal 14 through resistor R3, and current switching transistor Q5 has a base connected to clock input terminal 13a. In other words, current switching transistor Q5 is arranged for interposition in

15 first bypass path 20.

[0028]

As well, current source transistor Q7 has a base connected to voltage control circuit 18, and current source transistor Q7 has an emitter connected to low potential power supply terminal 15.

20 [0029]

On the other hand, data holding differential pair 17 includes transistors Q3 and Q4, wherein transistor Q3 has a collector connected to the collector of transistor Q1 and to data signal output terminal 12a, and transistor Q4 has a collector connected to the collector of transistor Q2 and

25 to data signal output terminal 12b, respectively. Also, transistor Q3 has a base connected to data signal output terminal 12b, and transistor Q4 has a

base connected to data signal output terminal 12a, respectively. Also, a common emitter of data holding differential pair 17, i.e., an emitter connection point of transistors Q3 and Q4, is connected to an emitter of current switching transistor Q6 and to a collector of current source transistor

5 Q8.

[0030]

Further, current switching transistor Q6 has a collector connected to high potential power supply terminal 14 through resistor R4, and current switching transistor Q6 has a base connected to clock input terminal 13b.

10 In other words, current switching transistor Q6 is arranged for interposition in second bypass path 21.

[0031]

Like wise, current source transistor Q8 has a base connected to voltage control circuit 19, and current source transistor Q8 has an emitter connected to low potential power supply terminal 15.

[0032]

Then, voltage control circuit 18 is configured to adjust the amount of current supplied to data reading differential pair 16 in accordance with the signal level of the clock signal. More specifically, voltage control circuit 18

20 adjusts the current level such that the amount of current supplied to data reading differential pair 16 when the signal level of the clock signal is at a low level is larger than the amount of current supplied to data reading differential pair 16 when the signal level is at a high level. In other words, a high potential level is applied to the base point of current source transistor Q7
25 when the clock signal is at a low level, while a low potential level is applied to the base point of current source transistor Q7 when the clock signal is at a

high level.

[0033]

Likewise, voltage control circuit 19 is configured to adjust the amount of current supplied to data holding differential pair 17 in accordance with the
5 signal level of the complementary clock signal. More specifically, voltage control circuit 19 adjusts the current level such that the amount of current supplied to data holding differential pair 17 when the signal level of the complementary clock signal is at a low level is larger than the amount of current supplied to data holding differential pair 17 when the signal level is at
10 a high level. In other words, voltage control circuit 19 applies voltage at a high potential level to the base point of current source transistor Q8 when the complementary clock signal is at a low level, and applies a low potential level to the base point of current source transistor Q8 when the complementary clock signal is at a high level.

15 [0034]

Next, the operation of the latch circuit of the first embodiment will be described with reference to Fig. 6.

[0035]

Since current switching transistor Q5 does not operate (off operation)
20 when the clock signal applied from clock signal input terminal 13a is at a low level, first bypass path 20 is opened (non-conducting state). Therefore, no current flows into first bypass path 20, and a current through current source transistor Q7 is completely supplied to data reading differential pair 16. In this event, voltage control circuit 18 applies the high potential level to the
25 base point of current source transistor Q7 in synchronization with the opened state of first bypass path 20. As a result, current source transistor Q7

supplies a sufficient amount of current to data reading differential pair 16.

[0036]

On the other hand, when the clock signal applied from clock signal input terminal 13a is at a high level, current switching transistor Q5 operates 5 (on operation), causing first bypass path 20 to close (conducting state). Therefore, a current supplied from current source transistor Q7 passes through first bypass path 20. In this event, voltage control circuit 18 applies voltage at a low potential level to the base point of current source transistor Q7 in synchronization with the closed state of first bypass path 20. As a 10 result, a reduced amount of current is supplied to data reading differential pair 16 by current source transistor Q7. This also restricts the amount of unwanted leak current which flows into data reading differential pair 16.

[0037]

For reference purposes, when the clock signal applied from clock 15 signal input terminal 13a is at a low level, the complementary clock signal applied from clock signal input terminal 13b is at a high level, so that current switching transistor Q6 operates (on operation), causing second bypass path 21 to close (conducting state). In this event, voltage control circuit 19 operates in a way that is opposite to the way that voltage control circuit 18 20 operates, i.e., applies a signal at a low potential level to the base point of current source transistor Q8. On the other hand, when the clock signal applied from clock signal input terminal 13a is at a high level, the complementary clock signal applied from clock signal input terminal 13b is at a low level, so that current switching transistor Q6 does not operate (off 25 operation), causing second bypass path 21 to open (non-conducting state). The operation of voltage control circuit 19 in this event is a reverse operation

to voltage control circuit 18, i.e., applies a signal at the high potential level to the base point of current source transistor Q8.

[0038]

As described above, according to the first embodiment, voltage
5 control circuit 18 or 19 applies, to the base point of current source transistor Q7 or Q8, voltage at a potential level which is high or low in synchronization with the opening/closing of bypass path 20 or 21 (in synchronization with the clock), so that the unwanted leak current can be automatically restrained from flowing into differential pairs 16 and 17 to realize a low-voltage latch
10 circuit with a high-margin which is free of data errors.

[0039]

Also, in order that a conventional parallelly arranged latch circuit operates correctly, the size of a current switching transistor must be larger than transistors which make up a data reading differential pair (or a data holding differential pair), for example, by a factor of approximately four, for purposes of providing a clock signal with an imposing force. In contrast, latch circuit 1a of the first embodiment can be operated correctly even when the size of current switching transistors (Q5, Q6) is limited to be larger than the transistors (Q1, Q2, Q3, Q4), which make up the differential pairs, by a
15 factor of approximately one to two. Further, since the transistor size can be limited, latch circuit 1a of the first embodiment can produce an increase in speed and a reduction in consumed current.
20

[0040]

(Second Embodiment)

25 A second embodiment implements voltage control circuits 18 and 19 in the first embodiment.

[0041]

Referring first to Figs. 7A, 7B, a description will be given of the configuration of a latch circuit of the second embodiment. In this regard, in the latch circuit of the second embodiment, similar components to those in the latch circuit of the first embodiment are designated the same reference numerals. In addition, the same descriptions are omitted.

[0042]

Figs. 7A, 7B illustrate circuit diagrams of the latch circuit of the second embodiment. In this regard, since data reading differential pair 16 has a circuit identical to the circuit of data holding differential pair 17 in the connection layout (substantially in bilateral symmetry), elements such as transistors in the circuit of data holding differential pair 17 are placed in parenthesis in the following description (the same applies to a third embodiment onward).

[0043]

As illustrated in Fig. 7A, in latch circuit 1b, voltage control circuit 18 (or 19) is disposed between the collector of current switching transistor Q5 (or Q6) and the base of current source transistor Q7 (or Q8), and has feedback path 22 (or 23) for applying information to the base of current source transistor Q7 (or Q8), about the signal level at the collector point of current switching transistor Q5 (or Q6). In this way, the amount of current supplied by current source transistor Q7 (or Q8) can be controlled in synchronization with the opening/closing of bypass path 20 (or 21), thus restricting unwanted leak current from flowing into differential pair 16 (or 17).

[0044]

Fig. 7B illustrates a specific example of voltage control circuits 18 and

19. Voltage control circuit 18 (or 19) comprises transistor Q9 (or Q10), transistor Q11 (or Q12), and the like. Transistor Q9 (or Q10) has a collector connected to high potential power supply terminal 14; a base connected to the collector of current switching transistor Q5 (or Q6); and an emitter to the 5 collector and the base of transistor Q11 (or Q12) through resistor R5 (or R6). Transistor Q11 (or Q12) in turn has the collector and base connected to the base of current source transistor Q7 (or Q8), and an emitter connected to low potential power supply terminal 15.

[0045]

10 Referring next to Fig. 7B, a description will be given of the operation of the latch circuit of the second embodiment.

[0046]

When the clock signal applied from clock signal input terminal 13a is at a low level, current switching transistor Q5 does not operate (off operation), 15 causing first bypass path 20 to open (non-conducting state), so that voltage at a high potential level is applied to the collector of transistor Q5, i.e., the base of transistor Q9 through resistor R3, resulting in an increase in the amount of current flowing into voltage control circuit 18. Thus, the potential level increases at the base and collector points of transistor Q11 in voltage control circuit 18, resulting in an increase in the amount of collector current of 20 current source transistor Q7 in the base point of which an input point is set at this point. In other words, voltage control circuit 18 applies the high potential level to the base point of current source transistor Q7 in synchronization with the opened state of first bypass path 20. As a result, 25 current source transistor Q7 supplies a sufficient amount of current to data reading differential pair 16.

[0047]

On the other hand, when the clock signal applied from clock signal input terminal 13a is at a high level, current switching transistor Q5 operates (on operation), causing first bypass path 20 to close (conducting state), so
5 that voltage at a low potential is applied to the base of transistor Q9 through resistor R3, resulting in a reduction in the amount of current flowing into voltage control circuit 18. Thus, the potential level decreases at the base and at the collector points of transistor Q11 in voltage control circuit 18, resulting in a reduction in the amount of collector current of current source
10 transistor Q7 in the base point of which an input point is set at this point. In other words, voltage control circuit 18 applies voltage at a low potential level to the base point of current source transistor Q7 in synchronization with the closed state of first bypass path 20. As a result, the amount of unwanted leak current is also restrained from flowing into data reading differential pair
15 16.

[0048]

For reference purposes, when the clock signal applied from clock signal input terminal 13a is at a low level, the complementary clock signal applied from clock signal input terminal 13b is at a high level, so that current switching transistor Q6 operates (on operation), causing second bypass path 21 to close (conducting state). The operation of voltage control circuit 19 (operation of transistor Q10 and transistor Q12) in this event is similar to the operation of voltage control circuit 18 (operation of transistor Q9 and transistor Q11) when the clock signal is at a high level. On the other hand,
20 25 when the clock signal applied from clock signal input terminal 13a is at a high level, the complementary clock signal applied from clock signal input terminal

13b is at a low level, so that current switching transistor Q6 does not operate (off operation), causing second bypass path 21 to open (non-conducting state). The operation of voltage control circuit 19 (operation of transistor Q10 and transistor Q12) in this event is similar to the operation of voltage control circuit 18 (operation of transistor Q9 and transistor Q11) when the clock signal is at a low level.

5 [0049]

Fig. 8A represents the manner in which current I1, which flows through the bypass path, and current I2, which flows through the differential pair, vary in synchronization with variations in the clock level (signal level) of the clock signal of Fig. 8B. As shown in Fig. 8A, it is understood that, as compared with the conventional latch circuit illustrated in Fig. 3, when the current switching transistor turns on to permit I1 to flow, current I2 is sufficiently restrained from flowing toward the differential pair to prevent 10 unwanted leak current from flowing.

15 [0050]

As described above, according to the second embodiment, in addition to the effects of the first embodiment, an unwanted leak current can be automatically restrained from flowing into the differential pair by feeding 20 information about the signal level at the collector point of the current switching transistor back to the base of the current source transistor.

[0051]

For reference purposes, latch circuit 1b described above can be applied to a variety of circuits. Figs. 9A, B illustrate master/slave D-type flip-flop circuits (F/F) which are used for identifiers and the like. In Fig. 9A, the 25 latch circuit is employed for both a master circuit and a slave circuit. On the

other hand, in Fig. 9B, a master circuit and a slave circuit share current switching transistors Q5 and Q6 and voltage control circuits 18 and 19 which make up the latch circuit.

[0052]

5 (Third Embodiment)

Referring first to Figs. 10A, B, a description will be given of the configuration of a latch circuit of a third embodiment. In this regard, in the latch circuit of the third embodiment, parts common to the latch circuits of the first or second embodiment are designated the same reference numerals.

10 In addition, the same descriptions are omitted.

[0053]

Figs. 10A, B illustrate circuit diagrams of the latch circuit of the third embodiment. As illustrated in Fig. 10A, latch circuit 2 comprises a level shift circuit in place of the voltage control circuit in the latch circuit described in the first or second embodiment. As compared with the latch circuit in the first or second embodiment, part of the circuit connections is different. In latch circuit 2 illustrated in Fig. 10A, current switching transistor Q5 has the base connected to clock input terminal 13a and to level shift circuit 24. Thus, a clock signal applied from clock input terminal 13a is branched into two lines which are fed to the base of current switching transistor Q5 and to level shift circuit 24. Then, level shift circuit 24 is connected to the base of current source transistor Q8.

[0054]

On the other hand, current switching transistor Q6 has the base connected to clock input terminal 13b and to level shift circuit 25. Thus, a complementary clock signal applied from clock input terminal 13b is

branched into two lines which are fed to the base of current switching transistor Q6 and to level shift circuit 25. Then, level shift circuit 25 is connected to the base of current source transistor Q7.

[0055]

5 In this way, similar to the first and second embodiments, the amount of current supplied by current source transistor Q7 (or Q8) can be controlled in synchronization with opening/closing of bypass path 20 (or 21), thus restraining unwanted leak current from flowing into differential pair 16 (or 17).

[0056]

10 For reference purposes, current source transistor Q7 and level shift circuit 25 function as first control means in the present invention, and current source transistor Q8 and level shift circuit 24 function as second control means in the present invention.

[0057]

15 Fig. 10B illustrates a specific example of level shifts 24 and 25. Level shift circuit 24 (or 25) comprises transistor Q13 (or Q14) and the like. Transistor Q13 (or Q14) has a collector connected to high potential power supply terminal 14; a base connected to the base of current switching transistor Q5 (or Q6); and an emitter connected to low potential power supply terminal 15 through resistor R7 (or R8), and also connected to the base of transistor Q8 (or Q7).

[0058]

Referring next to Fig. 10B, a description will be given of the operation of the latch circuit of the third embodiment.

25 [0059]

When a clock signal applied from clock signal input terminal 13a is at

a low level, current switching transistor Q5 does not operate (off operation), causing first bypass path 20 to open (non-conducting state). In this event, since a complementary clock signal applied from clock signal input terminal 13b is at a high level, an increased amount of current flows through transistor

5 Q14 and resistor R8 in level shift circuit 25. Thus, voltage at a high potential level is applied to the base point of current source transistor Q7, resulting in an increase in the amount of collector current of current source transistor Q7. In other words, level shift circuit 25 applies voltage at the high potential level to the base point of current source transistor Q7 in

10 synchronization with the opened state of first bypass path 20. As a result, current source transistor Q7 supplies a sufficient amount of current to data reading differential pair 16. For reference purposes, in this event, a reduced amount of current flows through transistor Q13 and resistor R7 in level shift circuit 24, with the result that voltage at a low potential level is applied to the

15 base point of current source transistor Q8.

[0060]

On the other hand, when the clock signal applied from clock signal input terminal 13a is at a high level, current switching transistor Q5 operates (on operation), causing first bypass path 20 to close (conducting state). In

20 this event, since the complementary clock signal applied from clock signal input terminal 13b is at a low level, a reduced amount of current flows through transistor Q14 and resistor R8 in level shift circuit 25. Thus, voltage at a low potential level is applied to the base point of current source transistor Q7, causing a reduction in the amount of collector current of

25 current source transistor Q7. In other words, level shift circuit 25 applies voltage at the low potential level to the base point of current source transistor

Q7 in synchronization with the closed state of first bypass path 20. As a result, the amount of unwanted leak current is also restrained from flowing into data reading differential pair 16. For reference purposes, in this event, an increasing amount of current flows through transistor Q13 and resistor R7 5 in level shift circuit 24, with the result that voltage at a high potential level is applied to the base point of current source transistor Q8.

[0061]

As described above, according to the third embodiment, even when a level shift circuit is used to build a circuit, unwanted leak current can be 10 automatically restrained from flowing into differential pairs 16 and 17 in a manner similar to the first and second embodiments.

[0062]

(Fourth Embodiment)

Referring to Figs. 11A, B, a description will be given of the 15 configuration of a latch circuit of a fourth embodiment. In this regard, in the latch circuit of the fourth embodiment, parts common to the latch circuit in the first or second embodiment are designated the same reference numerals. In addition, the same descriptions are omitted.

[0063]

Figs. 11A, B illustrate circuit diagrams of the latch circuit of the fourth 20 embodiment. As illustrated in Fig. 11A, in latch circuit 3, a circuit element having inductance component L and a circuit element having capacitance component C are connected in parallel to the collectors of current switching transistors Q5 and Q6.

25 [0064]

Here, the circuit element having inductance component L is

implemented by extending a wire between the collector point of current switching transistor Q5 (or Q6) and high potential power supply terminal 14, or by inserting herein a spiral inductor. On the other hand, circuit element 26 (or 27) having capacitance component C is implemented, for example, by 5 the voltage control circuit described in the second embodiment.

[0065]

Fig. 11B illustrates an example which employs the voltage control circuit for the circuit element having capacitance component C. In the latch circuit of the fourth embodiment, inductors L1, L2 are interposed between the 10 collector points of current switching transistors Q5, Q6 and high potential power supply terminal 14, through resistors R3, R4, respectively, and inductors are interposed between the collector of transistor Q1 and resistor R1 and between the collector of transistor Q2 and resistor R2, respectively. The rest of circuit configuration in latch circuit 3 is similar to latch circuit 1b 15 (Fig. 7B) in the second embodiment, and the operation of latch circuit 3 is also similar to the operation of latch circuit 1b of the second embodiment.

[0066]

Consequently, according to latch circuit 3 of the fourth embodiment, effects similar to those of latch circuit 1b can be provided. Specifically, 20 unwanted leak current can be automatically restrained from flowing into differential pairs 16 and 17.

[0067]

Further, according to latch circuit 3 of the fourth embodiment, an effect that improves high-speed performance is realized. Specifically, by inserting 25 inductors L1, L2 between the collector points of current switching transistors Q5, Q6 and high potential power supply terminal 14, as described above,

- parallel resonance arises between inductance component L added thereto and base-emitter capacitance Cbe possessed by transistor Q9 (or Q10) in voltage control circuit 26 (or 27). When a value is selected for component L that should be added with respect to the value of Cbe such that a resonance frequency appears in a desired high-frequency region, the gain can be increased in the desired high-frequency region. As a result, it is possible to improve the high-speed performance of the switching means (circuit unit) made up of transistors Q5, Q6, which receives a complementary clock signal to perform a current switching operation.
- 10 [0068]
- For reference purposes, the method of increasing the speed through the insertion of inductors has been conventionally and widely used in differential pairs 16 and 17. However, such a method has conventionally experienced difficulties in producing the foregoing effect when it is used in the switching circuit unit made up of transistors Q5, Q6 for performing the current switching operation. Specifically, since the output of the differential pair side is always applied to a transistor in a circuit at the next stage, as illustrated in Fig. 4, parallel resonance can be produced between capacitance Cbe possessed by the transistor and inserted inductor L, whereas there are no circuit elements, such as transistor having large capacitance component, that have not been conventionally connected to the output side of a switching circuit unit so that simple insertion of inductors does not lead to the resonance. In latch circuit 3 of this embodiment, since the voltage control circuit is connected to the output side (collector side of current switching transistor Q5, Q6) of the switching circuit unit, inserting inductor L can have the effect of improving high-speed performance.

[0069]

(Fifth Embodiment)

Referring to Figs. 12A, B, a description will be given of the configuration of a latch circuit of a fifth embodiment. In this regard, in the 5 latch circuit of the fifth embodiment, parts common to the latch circuit in the first or second embodiment are designated the same reference numerals. In addition, the same descriptions are omitted.

[0070]

Figs. 12A, B illustrate circuit diagrams of the latch circuit of the fifth 10 embodiment. As illustrated in Fig. 12A, in latch circuit 4, a circuit element having inductance component L and a circuit element having capacitance component C are connected in series to the collectors of current switching transistors Q5 and Q6.

[0071]

15 Here, the circuit element having inductance component L is implemented by extending a wire between the collector point of current switching transistor Q5 (or Q6) and high potential power supply terminal 14, or by inserting herein a spiral inductor. On the other hand, the circuit element having capacitance component C is implemented, for example, by 20 the voltage control circuit described in the second embodiment.

[0072]

Fig. 12B illustrates an example which employs the voltage control circuit for the circuit element having capacitance component C. In latch circuit 4 of the fifth embodiment, inductors L3, L4 are interposed between the 25 collector points of current switching transistors Q5, Q6 and the base points of transistors Q9, Q10 in voltage control circuits 26, 27, respectively, and

inductors are interposed between the collector of transistor Q1 and resistor R1 and between the collector of transistor Q2 and resistor R2, respectively. The rest of the circuit configuration in latch circuit 4 is similar to latch circuit 1b (Fig. 7B) in the second embodiment. The operation of latch circuit 4 is
5 also similar to the operation of latch circuit 1b of the second embodiment.

[0073]

Consequently, according to latch circuit 3 of the fourth embodiment, effects similar to those of latch circuit 1b can be provided. Specifically, unwanted leak current can be automatically restrained from flowing into
10 differential pairs 16 and 17.

[0074]

Further, according to latch circuit 4 of the fifth embodiment, has the effect of improving high-speed performance. Specifically, by inserting inductors L3, L4 between the collector points of current switching transistors
15 Q5, Q6 and the base points of transistors Q9, Q10, respectively, as described above, serial resonance arises between inductance component L added thereto and base-emitter capacitance Cbe possessed by transistor Q9 (or Q10) in voltage control circuit 26 (or 27). When a value is selected for component L that should be added respect to the value of Cbe such that a
20 resonance frequency appears in a desired high-frequency region, the gain can be increased in the desired high-frequency region. As a result, it is possible to improve the high-speed performance of the switching means (circuit unit) made up of transistors Q5, Q6, which receives a complementary clock signal to perform a current switching operation.

25 [0075]

(Sixth Embodiment)

Referring to Fig. 13, a description will be given of the configuration of a latch circuit of a sixth embodiment. In this regard, in the latch circuit of the sixth embodiment, parts common to the latch circuit in the first or second embodiment are designated the same reference numerals. In addition, the 5 same descriptions are omitted.

[0076]

Fig. 13 illustrates a circuit diagram of the latch circuit of the sixth embodiment. Latch circuit 5 comprises output terminals 16a, 16b for sending a clock signal to the other logic circuit (for example, a functional 10 circuit such as a flip-flop circuit) 6, and current switching transistors Q5, Q6 have their collectors connected to output terminals 16a, 16b, respectively. Then, output terminals 16a, 16b are connected to clock input terminals of the other logic circuit 6. In this way, latch circuit 5 can send a complementary 15 clock signal (information on the signal level at the collectors of current switching transistors Q5, Q6) to the other logic circuit 6 through output terminals 16a, 16b, while simultaneously functioning essentially as a latch circuit. For reference purposes, voltage control circuits 18, 19, described in the first embodiment, are connected to the bases of current source transistors Q7, Q8, respectively.

20 [0077]

Fig. 14A is a circuit block diagram of 2:1 MUX which is built using latch circuits 5 illustrated in Fig. 13. In Fig. 14A, all or part of master/slave type flip-flop circuit (MS-F/F) 7, master/slave/master type flip-flop circuit (MSM-F/F) 8, and selector circuit (SELECTOR) 9 are built using latch circuit 25 5 illustrated in Fig. 13.

[0078]

Therefore, according to the circuit blocks illustrated in Fig. 14A, a complementary clock signal need not be supplied to respective circuit elements through independent paths, as the circuit blocks of conventional 2:1 MUX illustrated in Fig. 5, but the respective circuit elements can be connected in series without branching a clock signal path into a large number of paths. Accordingly, since no buffer circuit (BUF) is required on each branch for signal amplification, the number of buffer circuits can be largely reduced which consequently provides a large reduction in power consumption.

10 [0079]

While the foregoing has shown an example in which latch circuit 5 illustrated in Fig. 14A is applied to 2:1 MUX, the present invention is not only limited to this configuration, but can also be applied, for example, to overall circuit blocks illustrated in Fig. 14B.

15 [0080]

While the first to sixth embodiments described above have shown examples in which the current supply control circuit of the present invention is mainly applied to a latch circuit, the present invention is not only limited to this configuration, but can be applied to any semiconductor integrated circuit 20 as a basic element circuit for a variety of logic circuits, for example, a data read circuit having a differential circuit, a selector circuit, and the like. In the following, referring to Fig. 15, a description will be given of an example in which the current supply control circuit of the present invention is applied to a selector circuit.

25 [0081]

Fig. 15 illustrates a circuit diagram of a selector circuit to which the

current supply control circuit of the present invention is applied. In this regard, while selector circuit 10 illustrated in Fig. 15 is slightly different from connections in latch circuit 1b illustrated in Fig. 7B, circuit components such as transistors, resistors and the like are the same, so that they are
5 designated the same reference numerals. In addition, the same descriptions are omitted.

[0082]

As illustrated in Fig. 15, selector circuit 10 includes first data reading differential pair 16 as a first differential circuit for reading first data signals
10 applied from first data signal input terminals 11a and 11b; second data reading differential pair 17 as a second differential circuit for reading second data signals applied from second data signal input terminals 11c and 11d; voltage control circuit 18 and current source transistor Q7 as first control means for controlling the amount of current supplied to first data reading differential pair 16; voltage control circuit 19 and current source transistor Q8 as second control means for controlling the amount of current supplied to second data reading differential pair 17; first bypass path for bypassing current around first data read differential pair 16; second bypass path 21 for bypassing current around second data reading differential pair 17; current
15 switching transistor Q5 as first switching means for opening/closing first bypass path 20 in accordance with the signal level of a clock signal applied from clock signal input terminal 13a; and current switching transistor Q6 as second switching means for opening/closing second bypass path 21 in accordance with the signal level of a complementary clock signal applied
20 from clock signal input terminal 13b.
25

[0083]

For reference purposes, bypass path 20, current switching transistor Q5, voltage control circuit 18, and current source transistor Q7 (or bypass path 21, current switching transistor Q6, voltage control circuit 19, and current source transistor Q8) function as the current supply control circuit of

5 the present invention.

[0084]

In selector circuit 10, first data reading differential pair 16 fetches a first data complementary signal in synchronization with the clock signal, second data reading differential pair 17 fetches a second data

10 complementary signal in synchronization with the complementary clock signal, and the first and second data complementary signals are alternately delivered from data signal output terminals 12a, 12b, wherein the current supply control circuit of the present invention is applied, thereby producing effects similar to the first and second embodiments.

15 [0085]

Alternatively, the foregoing selector circuit 10 may be built in a circuit configuration as illustrated in the aforementioned third to sixth embodiments, in which case effects similar to those in the third to sixth embodiments can be produced.

20 [0086]

Also, while the foregoing embodiments have been described on the assumption that bipolar transistors are representative of active elements, the present invention is not limited to any type of active elements, but can be applied similarly, for example, to such elements as FETs. Also, while the

25 transistors shown in Fig. 6 and the like apply npn-type transistors, pnp-type transistors may be employed instead.